What is claimed is:

[Claim 1] 1. A method for increasing the flexibility of placement of primary fuse macros on a microchip, comprising the steps of:

providing components of a fuse domain, said components comprising

one or more primary fuse macros,

overhead associated with said one or more primary fuse macros, and

one or more primary FSOURCE interface port structures;

arranging said components on said microchip such that at least one of said one or more primary fuse macros is located excessively distal from said one or more primary FSOURCE interface port structures; and

providing at least one supplemental FSOURCE interface port structure, said at least one supplemental FSOURCE interface port structure being proximate to and operatively connected to said one or more excessively distal primary fuse macros.

[Claim 2] 2. The method of claim 1, wherein said overhead comprises:

a fuse controller,

one or more secondary fuse macros, and

one or more tertiary fuse macros.

[Claim 3] 3. The method of claim 1 wherein said one or more primary FSOURCE interface port structures and said at least one supplemental FSOURCE interface port structure is a C4 pad.

[Claim 4] 4. The method of claim 1 wherein said one or more primary FSOURCE interface port structures and said at least one supplemental FSOURCE interface port structure is a wire bond pad.

[Claim 5] 5. The method of claim 1, wherein said fuse domain components comprise 64 primary fuse macros, 4 secondary fuse macros, and 2 tertiary fuse macros.

[Claim 6] 6. The method of claim 1 wherein said at least one supplemental FSOURCE interface port structure is operatively connected to a plurality of excessively distal primary fuse macros.

[Claim 7] 7. A microchip, comprising:

components of a fuse domain, said components comprising

one or more primary fuse macros,

overhead associated with said one or more primary fuse macros, and

one or more primary FSOURCE interface port structures;

wherein at least one of said one or more primary fuse macros is located excessively distal from said one or more primary FSOURCE interface port structures, and

at least one supplemental FSOURCE interface port structure, said at least one supplemental FSOURCE interface port structure being proximate to and operatively connected to said one or more excessively distal primary fuse macros.

[Claim 8] 8. The microchip of claim 7, wherein said overhead comprises:

a fuse controller,

one or more secondary fuse macros, and

one or more tertiary fuse macros.

[Claim 9] 9. The microchip of claim 7, wherein said one or more primary FSOURCE interface port structures and said at least one supplemental FSOURCE interface port structure is a C4 pad.

[Claim 10] 10. The microchip of claim 7, wherein said one or more primary FSOURCE interface port structures and said at least one supplemental FSOURCE interface port structure is a wire bond pad.

[Claim 11] 11. The microchip of claim 7, wherein said fuse domain components comprise 64 primary fuse macros, 4 secondary fuse macros, and 2 tertiary fuse macros.

[Claim 12] 12. The microchip of claim 7, wherein said at least one supplemental FSOURCE interface port structure is operatively connected to a plurality of excessively distal primary fuse macros.

[Claim 13] 13. A method for blowing fuses within a fuse domain in parallel, comprising the steps of

providing components of a fuse domain, said components comprising:

one or more primary fuse macros,

overhead associated with said one or more primary fuse macros, and

one or more primary FSOURCE interface port structures;

arranging said components on said microchip such that at least one of said one or more primary fuse macros is located excessively distal from said one or more primary FSOURCE interface port structures; and

providing at least one supplemental FSOURCE interface port structure, said at least one supplemental FSOURCE interface port structure being proximate to and operatively connected to said one or more excessively distal primary fuse macros simultaneously blowing at least two fuses of the fuse domain, wherein each of said at least two fuses is operatively connected to a different FSOURCE interface port structure within the domain.

[Claim 14] 14. The method of claim 13, wherein said overhead comprises:

a fuse controller,

one or more secondary fuse macros, and

one or more tertiary fuse macros.

[Claim 15] 15. The method of claim 13 wherein said one or more primary FSOURCE interface port structures and said at least one supplemental FSOURCE interface port structure is a C4 pad.

[Claim 16] 16. The method of claim 13 wherein said one or more primary FSOURCE interface port structures and said at least one supplemental FSOURCE interface port structure is a wire bond pad.

[Claim 17] 17. The method of claim 13, wherein said fuse domain components comprise 64 primary fuse macros, 4 secondary fuse macros, and 2 tertiary fuse macros.

[Claim 18] 18. The method of claim 13 wherein said at least one supplemental FSOURCE interface port structure is operatively connected to a plurality of excessively distal primary fuse macros.

[Claim 19] 19. An integrated circuit comprising:

a domain of functional elements including

a circuit to said functional elements

a first off-chip connection for said domain of functional elements

wherein at least one of said functional elements is excessively distal from said first off-chip connection, and

a second off-chip connection proximal to said at least one functional element which is excessively distal from said first off-chip connection.

[Claim 20] 20. The integrated circuit of claim 19, wherein said functional elements are primary fuse macros.

[Claim 21] 21. The integrated circuit of claim 19 wherein said first and second off-chip connections are FSOURCE interface port structures.